REMARKS

This is a full and timely response to the final Office Action (Paper No. 5) mailed by the U.S. Patent and Trademark Office on ***May 17, 2002***. Upon entry of the foregoing amendments, claims 1-7 and 10-26 remain pending in the present application. Claims 1, 6, 10, and 11 have been amended and claims 8 and 9 have been canceled. It is believed that the foregoing amendments add no new matter to the present application. In view of the foregoing amendments and the following remarks, reconsideration and allowance of the present application and pending claims are respectfully requested.

Applicants would like to thank Examiner Kumar for the time spent during a telephone conversation with Applicants' representative on July 17, 2002. During that conversation, the *McMahan et al.* reference (U.S. Patent No. 5,870,446) was discussed, particularly the clocking signals of *McMahan et al.* The differences between *McMahan et al.* and the present invention were also addressed.

Applicant would also like to thank Examiner Kumar for pointing out allowable subject matter in the final office action, wherein claims 5, 9, 10, and 14-26 were indicated as allowable if written in independent form incorporating the limitations of the base claim and intervening claims. In response to this indication of allowable subject matter, claim 6 has been amended to incorporate the limitations of claim 9 and intervening claim 8. Thus, independent claim 6 and the dependent claims 7, 10, 23, and 24 that depend from claim 6, are believed to be allowable.

During the telephone interview, the Examiner suggested that if a claim element were added to the independent claims such that the master clock signal is defined by a frequency that is an integer multiple of the frequency of the circuit clocking signal, then the claim would

distinguish further from the prior art. Therefore, to clarify that the master clock is an integer multiple of the circuit clocking signal, claims 1 and 11 have been amended to include such an aspect. Particularly, the master clock signal is now defined as ***"having a frequency that is an integer multiple"*** of the frequency of the DCE clocking signal. Since the circuit clocking signal has the same frequency as the DCE clocking signal, it naturally follows that master clock signal is an integer multiple of the circuit clocking signal. In contrast to the present claims, the clocking signals of *McMahan et al.* are not integer multiples of each other.

Rejections Under 35 U.S.C. § 102(e)

Since claims 8 and 9 have been cancelled, the 35 U.S.C. 102(e) rejection of these claims is considered moot. Since claim 6 has been amended to incorporate the subject matter of claims 8 and 9, which the Examiner has indicated as allowable subject matter, the rejection of claim 6 is considered moot. Applicants submit that dependent claims 7, 10, 23, and 24 are allowable for at least the reason that they depend from allowable independent claim 6. *In re Fine* 837 F.2d 1071, 5 USPQ 2d 1596, 1598 (Fed. Cir. 1988).

Claim 1:

Claim 1 has been amended to further define the master clock signal as ***"having a frequency that is an integer multiple"*** of the frequency of the circuit clocking signal. *McMahan et al.* teaches a master clock signal having a frequency of 16 MHz and a TX clock signal having a frequency of 1.544 MHz. Therefore, the master clock signal of *McMahan et al.* is not an integer multiple of the TX clock signal. Anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. See *In re*

Paulsen, 30 F.3d 1475, 31 USPQ 2d 1671 (Fed. Cir.1994) and *In re Spada*, 911 F.2d 705, 15 USPQ 2d 1655 (Fed. Cir. 1990).

Furthermore, Applicants assert that *McMahan et al.* does not teach or suggest the claimed element of the clock generator ***"deriving a circuit clocking signal from said master clock signal."*** The clock generator 55 of *McMahan et al.* instead receives a logic signal from the phase generator 51 selecting either a normal clock signal TX CK or an inverted clock signal TX CK BAR. See col. 5, lines 54-60. Applicants assert that *McMahan et al.* is silent as to the aspect of deriving either the normal clock signal TX CK or inverted clock signal TX CK BAR from the master clock signal and respectfully request that the Examiner specifically point out the passage in *McMahan et al.* that teaches or suggests such an aspect.

Claim 1 has been further amended to include the aspect that the first sample enable signal is generated at a first time that is ***"related to said circuit clocking signal"*** and that the second sample enable signal is generated at a second time that is ***"related to said master clock signal."*** Support for these claim elements can be found in Figs. 4 and 5 showing the sample enable generator 34 generating the two sample enable signals along lines 35 and 36 from the master clock signal and the circuit clocking signal. Support can also be found in the specification corresponding to these figures. *McMahan et al.* does not teach or suggest that the data sampling shift register 15 has a first signal at a first time ***"related to said circuit clocking signal"*** and a second signal at a second time ***"related to said master clock signal."*** For at least these reasons, Applicants assert that claim 1 is allowable and that dependent claims 2-5 and 16-22 are allowable for at least the reason that they depend from allowable claim 1. *In re Fine, supra.*

Claim 11:

Claim 11 has been amended to include that the master clock signal has a frequency ***"that is an integer multiple"*** of the frequency of the DCE clocking signal, which has the same frequency as the circuit clocking signal. As mentioned above with respect to claim 1, *McMahan et al.* teaches uses clocking signals that are not integer multiples. Furthermore, *McMahan et al.* does not include the claimed element of ***"deriving a circuit clocking signal from said master clock signal."***

Applicants contend that claim 11 is further distinguished from *McMahan et al.* based on the claim element of obtaining the first sample at a first time ***"based on said circuit clocking signal"*** and the second sample at a second time ***"based on said master clock signal."*** *McMahan et al.* does not disclose, teach, or suggest obtaining sample of the DTE data signal based on the two clocking signals since *McMahan et al.* teaches only one clock signal HS CLK at the input of the data sampling shift register 15. The other clocking signal TX CLOCK from the clock generator 55 is never input into the data sampling shift register 15, nor would one of ordinary skill in the art be inclined to interpret *McMahan et al.* in such a manner.

CONCLUSION

For at least the foregoing reasons, Applicants respectfully request that all outstanding rejections be withdrawn and that all pending claims of this application be allowed to issue. If the Examiner has any comments regarding Applicants' response or intends to dispose of this matter in a manner other than a notice of allowance, Applicants request that the Examiner telephone Applicants' undersigned attorney.

Respectfully submitted,

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ANNOTATED VERSION OF MODIFIED CLAIMS
TO SHOW CHANGES MADE

In accordance with 37 C.F.R. § 1.121, please find below the amended claims in which the inserted language is underlined ("__") and the deleted language is enclosed in brackets ("[ ]"):

1. (Twice amended). A circuit for detecting errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal[,] in a communication environment wherein the DCE interfaces the DTE to a communication channel at an interface rate determined by the DCE clocking signal, the circuit comprising:

a master clock producing a master clock signal having a frequency that is an integer multiple of [greater than] the frequency of the DCE clocking signal;

a clock generator deriving a circuit clocking signal from said master clock signal, said circuit clocking signal having the same frequency as the DCE clocking signal;

a sample enable generator for generating a first sample enable signal at a first time related to said circuit clocking signal and a second sample enable signal at a second time related to said master clock signal; and

a sample comparator for using said first sample enable signal, said second enable signal and said DTE data signal to determine whether the DTE data signal has undergone a transition during the time interval between said first time and said second time.

6. (Twice amended). A circuit for detecting errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal[,] in a communication environment wherein the DCE interfaces the DTE to a communication channel, the circuit comprising:

means for producing a master clock signal having a frequency greater than the frequency of the DCE clocking signal;

means for deriving a circuit clocking signal from said master clock signal, said circuit clocking signal having the same frequency as the DCE clocking signal;

means for obtaining a first sample of said DTE data signal at a first time and means for obtaining a second sample of said DTE data signal at a second time, said second time being subsequent to said first time, the interval between said first time and said second time being less than the period of the DCE clocking signal; [and]

means for comparing said first sample to said second sample;

means for generating a selector control signal if said first sample is different from said second sample;

means for inverting said circuit clocking signal to produce an inverted circuit clocking signal; and

means for selecting an output signal from the group consisting of said circuit clocking signal and said inverted circuit clocking signal, in response to said selector control signal.

10. (Twice amended). The circuit of claim [9] 6, further comprising:

means for latching said DTE data signal.

11. (Twice amended). A method for detecting errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal[,] in a communication environment wherein the DCE interfaces the DTE to a communication channel, the method comprising the steps of:

providing a master clock signal having a frequency [greater than] that is an integer multiple of the frequency of the DCE clocking signal;

deriving a circuit clocking signal from said master clock signal, said circuit clocking signal having the same frequency as the DCE clocking signal;

obtaining a first sample of said DTE data signal at a first time based on said circuit clocking signal and a second sample of said DTE data signal at a second time based on said master clock signal, said second time being subsequent to said first time, the interval between said first time and said second time being less than the period of the DCE clocking signal; and

comparing said first sample to said second sample.